CLAIMS

1. A programmable logic device (PLD) including a plurality of logic array blocks (LAB's) connected by a PLD routing architecture, wherein at least one LAB is configured to determine a compression of a plurality of N-bit numbers, the one LAB comprising:

a plurality of look-up table (LUT) logic cells, each look-up table (LUT) logic cell configured to input three signals at three respective inputs of that look-up table (LUT) logic cell and to output two signals at two respective outputs of that look-up table logic cell (LUT) that are a sum and carry signal resulting from adding the three input signals;

input lines configured to receive input signals from the PLD routing architecture that represent the plurality of N-bit numbers and output lines configured to provide output signals to the PLD routing architecture that represent the compression of the plurality of N-bit numbers; and

LAB internal routing logic, not part of the routing architecture of the PLD, connecting the LUT logic cells such that the LUT logic cells collectively process the input signals, received at the input lines, that represent the N-bit numbers to generate the output signals, provided at the output lines, that represent the sum of the N-bit numbers.

2. The PLD of claim 1, wherein:

the LUT logic cells are organized into slices, each slice performing processing relating to a separate one of the bits of the N-bit numbers.

3. The PLD of claim 1, wherein:

each of the input lines is configured to receive one bit of one of the N-bit numbers.

4. The PLD of claim 1, wherein:

at least some of the input lines are configured to receive more than one bit of the plurality of N-bit numbers.

5. A programmable logic device, including a portion configured to determine the sum of at least four N-bit numbers having bit positions 1 through N, wherein:

the portion comprises a plurality of logic cells organized into a first stage and a second stage,

the first stage is organized into N logic cells that collectively operate as a carry-save adder, each of the N logic cells in the first stage being configured to receive a bit at a corresponding bit position of first, second and third of the four N-bit numbers, respectively, at three inputs of the logic cell and to provide a sum bit and carry bit for the corresponding bit position at two outputs of the logic cell, and

the second stage is organized into N logic cells, each of the N logic cells in the second stage being configured to receive, for a corresponding bit position, the sum bit from the logic cell for that corresponding bit position in the first stage, the bit for that bit position of the fourth operand, and the carry bit from the logic cell from the previous bit position in the first stage, and to provide a sum bit and carry bit for the corresponding bit position at two outputs of the logic cell; and

the sum bit and carry bit provided from all of the bit positions of the second stage collectively determine the sum of the at least four N-bit numbers.